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SUMMARY

Over 35 years of low-level development experience on CPU simulators, compilers, reverse engineering, emulating legacy computers, and performance tuning. I've blogged and published papers on CPU architecture, techniques for implementing fast emulators, and argued the case for binary translation based PCs. I have 14 U.S. patents granted to date related to emulation and virtulization. In the 1990's I developed the only commercial Apple Macintosh emulator for Windows PCs, "SoftMac", almost a decade before Apple themselves made the switch to Intel CPUs in 2006.

Since 2015, implemented Microsoft's Intel x86/x64 emulators for Windows on ARM, co-authored numerous patents, and helped realize the emulation based world on top of RISC silicon that I envisioned over 10 years ago.

WORK EXPERIENCE

Microsoft Corporation, Redmond WA, 2015 to 2022
- Development and productization of Microsoft's "xtajit" Intel x86 emulator for Windows on ARM
- Key designer of the 64-bit x64 emulation and "ARM64EC" emulation compatible ARM64X hybrid binaries
- Developer of the "xtabase" x64 refrence emulator and the Windows 11 "soft intrinsics" for ARM64EC
- Design and development of the native ARM32 and ARM64 tracing modes for Time Travel Debugging
- See U.S. patents # 11593113 11403100 11366666 11231918 11042422 10481999 10261785 10198341

Amazon Web Services, Seattle WA, 2013 to 2015
- Principal Engineer in AppStream, optimizing the streaming of Windows Direct3D applications from EC2
- Involved in performance analysis on recent Windows 2012 R2 instances and C4 (Xeon-v3 based) instance types
- Maintaining and optimizing the existing Android application streaming product called "Test Drive"
- Design and development of a high-performance ARM/Thumb emulation engine
- Presenting engineering talks on the topics of code optimization for AVX2 and scalable cloud emulation

Microsoft Corporation, Redmond WA, 2011 to 2013
- Developer on Visual Studio 2013 C/C++ backend team targetting ARM optimizations and new AVX2 extensions
- Bringup of the native C# compiler backend for the new ".NET Native"
- Redesigned the legacy iDNA instrumentation engine and prototyped a new faster binary translator

Amazon Web Services, Seattle WA, 2010 to 2011
- Principal Engineer in EC2 focusing on performance and correctness of Windows instances on the EC2 cloud
- Fixed serious issues relating to interrupt latency, clock drift, device drivers, and Windows guest VM performance
- Shipped two product releases: Windows 2008 R2 guest VM support, and cc2.8xlarge 16-core HPC instance
- Developed techniques and new tools to discover and monitor performance anomalies
- On-site customer engagement and contributing customer-facing documentation to the Amazon EC2 web site
- Co-inventor of U.S. patent #8935699 related to virtual machine scheduling and performance

Intel Corporation, Redmond WA and Santa Clara CA, 2008 to 2010
- First full-time engineer hired into the newly formed Hybrid Parallel Computing group at Intel
- Designed and developed simulation tools for performance analysis and new instruction modelling
- Participated in the hardware/software co-design of future Intel processors and new instruction set extensions
- Co-authored CGO and ISCA conference workshop papers related to the simulation work
- Co-inventor on several patents related to hardware transactional memory

Microsoft Corporation, Redmond WA, 2001 to 2008
- Lead developer on “Nirvana”, a dynamic recompilation instrumentation framework used by “iDNA”
- Co-authored paper on Nirvana and iDNA Time Travel Debugging technology published at VEE 2006
- Co-inventor on U.S. patent #7620938 relating to my work on iDNA Time Travel Debugging technology
- Lead developer on “Helium” Pentium III on 64-bit PowerPC emulation project for Xbox 360
- Co-inventor on U.S. patent #7752028 relating to simulation of arithmetic flags on PowerPC processors
- Maintenanced Vulcan and BBT (Microsoft’s static code instrumentation and optimization tools)
- Performance tuning ARM code on Windows Phone, PowerPC code on Xbox 360, and x86/x64 code on Windows

Emulators.com, Bellevue WA, 1997 to 2001 full time, ongoing hobby from 1988 to present
- Founded company to provide products related to Macintosh-PC cross-platform operability
- Designed, developed, and shipped the “SoftMac” Apple Macintosh emulator for Windows in under two years
- Negotiated distribution deals of SoftMac with resellers in Japan, Europe, and North America
- Managed and coordinated company exhibits at Macworld, Comdex, PC Expo, and CeBIT trade shows
- Customers include Microsoft, Honeywell, various school boards, and thousands of Apple and Atari end-users
- Blogger since 2000, helping PC users with their problems, posting hardware reviews and industry analysis
- Released much of our code as open source, and contributed to open source projects such as “Bochs” x86 emulator

Microsoft Corporation, Redmond WA, 1990 to 1997
- Full-time SDE in the Applications and Languages Divisions, focusing on performance issues and code quality
- Contributed to Visual C++ 4.x and 5.0 back end code generation optimizations producing 10% smaller code
- Design and developed the PowerPC P-code VM and bytecode instruction set used for Mac Office 98
- Boot-time and performance optimization work on Office 95, Office 97, Mac Office 98
- Also worked on Works for Windows 2.0, PC Works 3.0, POSIX runtimes in NT, and MASM for PowerPC

Microsoft Corporation, Redmond, WA, 1987 to 1989
- Three internships in the Applications Division on projects such as Multiplan for OS/2 and PowerPoint 2.0
- Used cross-platform development tools hosted on XENIX/386 and OS/2

EDUCATION

University of Waterloo, Waterloo, Ont., 1985 to 1990
- B.A. in Computer Engineering co-op program
- Awarded Engineering Faculty Special Entrance Scholarship (one of top 8 scholarships awarded per year)
- Ranked in top 16 students nationwide in various Canadian math and physics high school contests

SKILLS AND INTERESTS

- Proficient in C as well as x86/AMD64/Intel64, PowerPC, 680x0, 6502, and ARM32/ARM64 assembly languages
- Windows NT/XP/7/8/10/11, Windows 9x, MS-DOS, Mac OS, GEM/TOS, Fedora, RHEL, and Ubuntu operating systems
- Strong interests in mathematics, physics, electronics, and microprocessor architecture
- Experienced with public presentations, press interviews on television, radio, and magazines
- Authored numerous computer magazine articles since 1985, online hardware reviews, and years of blogging
- Open source contributions, including significant optimizations to the Bochs x86 simulator

PUBLICATIONS

“How Bochs Works”, June 2012
http://bochs.sourceforge.net/How%20the%20Bochs%20works%20under%20the%20hood%202nd%20edition.pdf

“Fast Microcode Interpretation with Transactional Commit/Abort”, AMAS-BT workshop at ISCA, San Jose, June 2011
http://www.emulators.com/docs/amas-bt2011.pdf

"Proposal for Hardware-Assisted Arithmetic Overflow Detection", WISH workshop at CGO, Toronto, April 2010
http://www.emulators.com/docs/LazyOverflowDetect_Final.pdf

"Virtualization without Direct Execution", AMAS-BT workshop at ISCA 2008, Beijing, June 2008
http://www.emulators.com/docs/VirtNoJit_Paper.pdf

"Framework for Instruction-level Tracing and Analysis", VEE 2006, Ottawa, June 2006
http://www.usenix.org/events/vee06/full_papers/p154-bhansali.pdf